EDSAC in Verilog

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EDSAC Replica Project

Initial Task: Reconstruct and Validate Logic

Starting point: Edsac Report - 1948

Mostly text, few diagrams

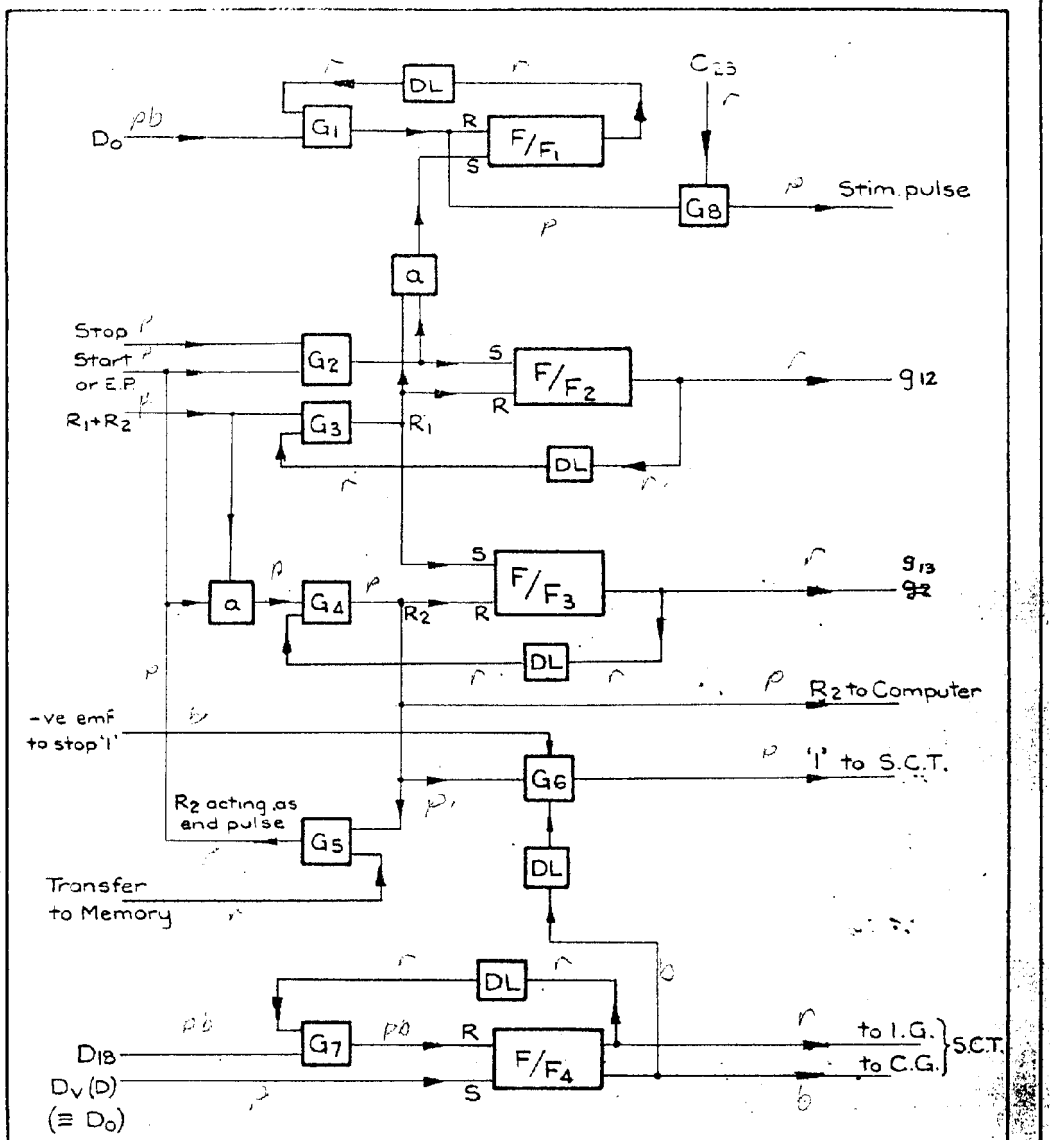
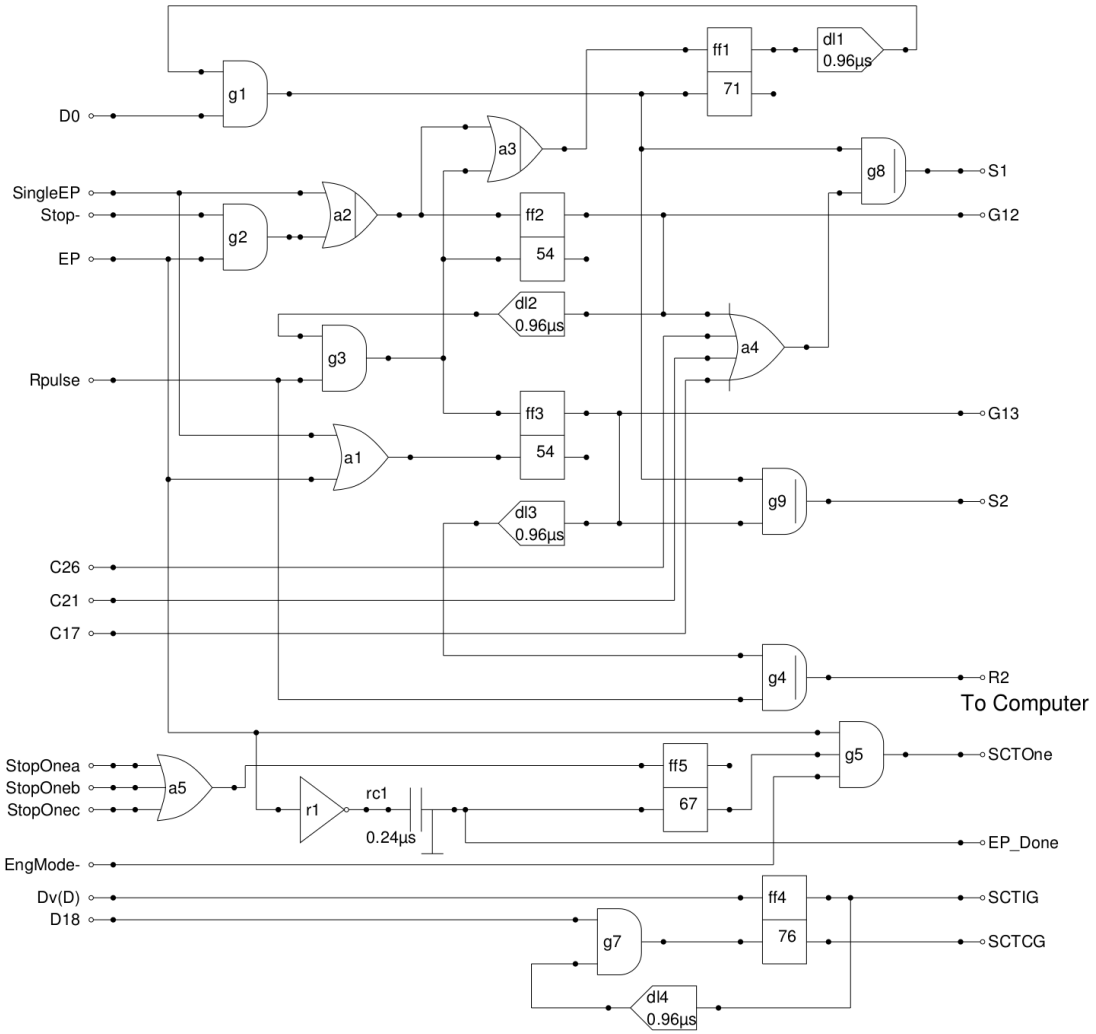


Fig. 7 Main Control Unit

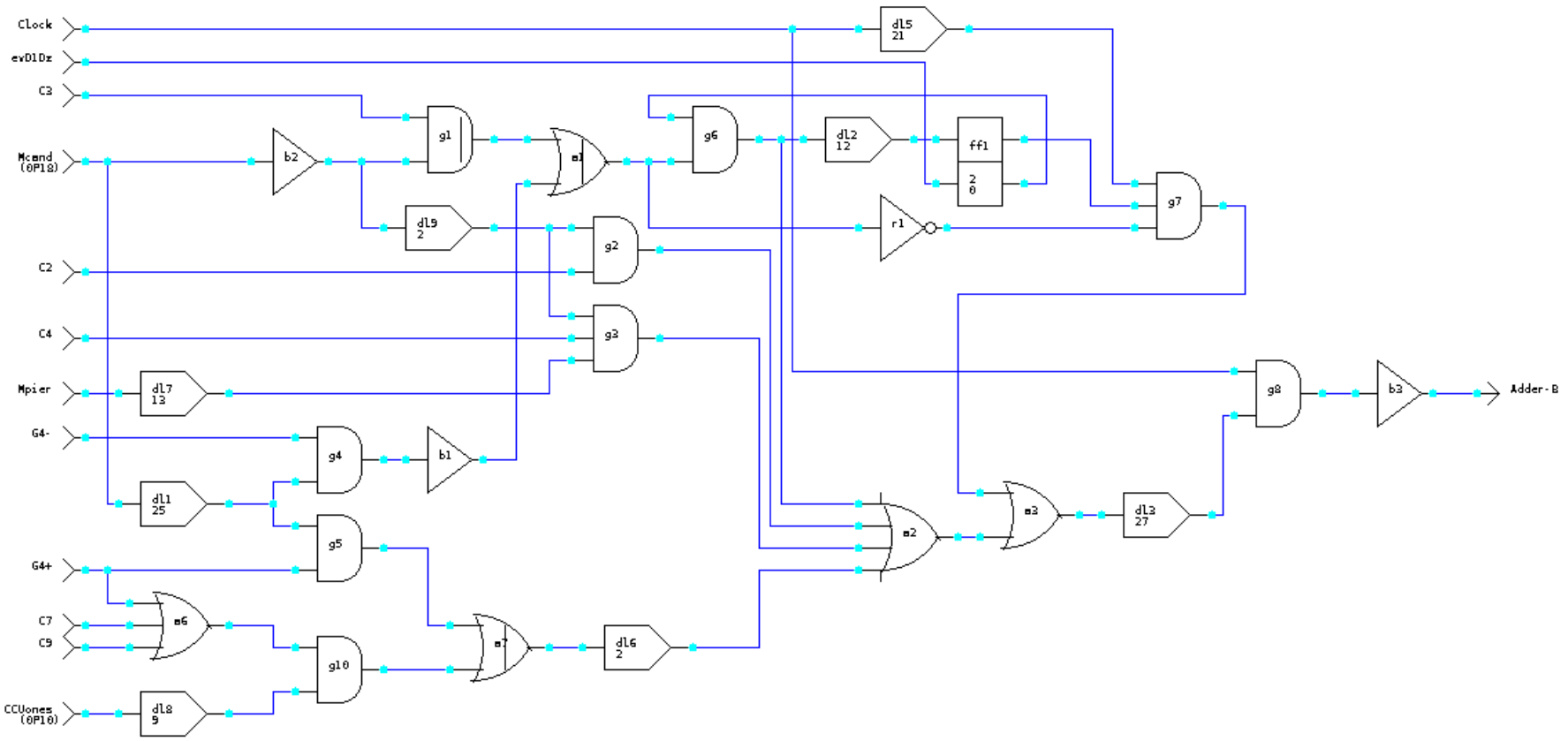
Redraw using a home-grown Logic Editor - ELSIE



MAIN CONTROL UNIT

Elsie4.2: CmpCol/R3P10+11

File Insert Action Modules Help



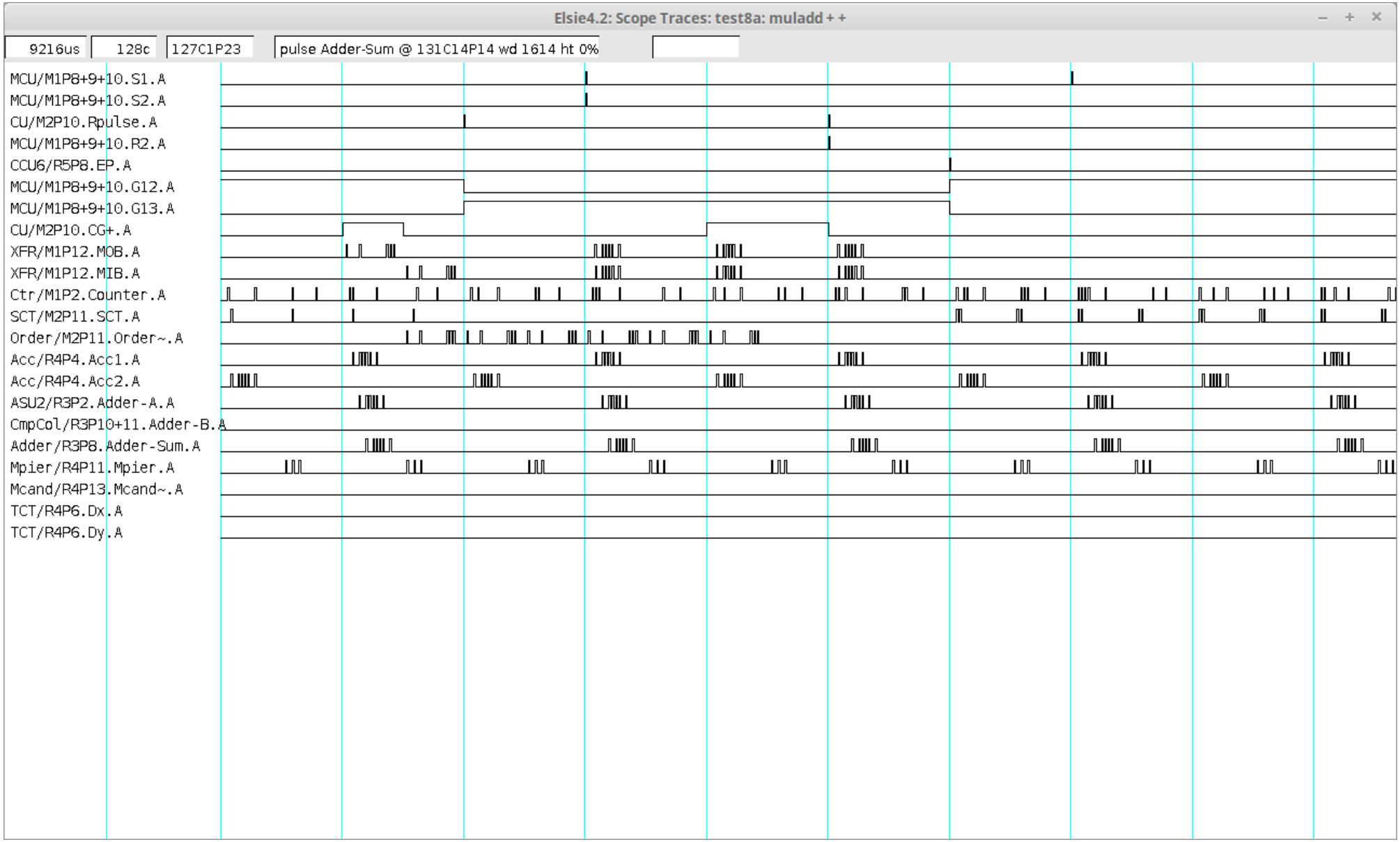
Complementer - Collater

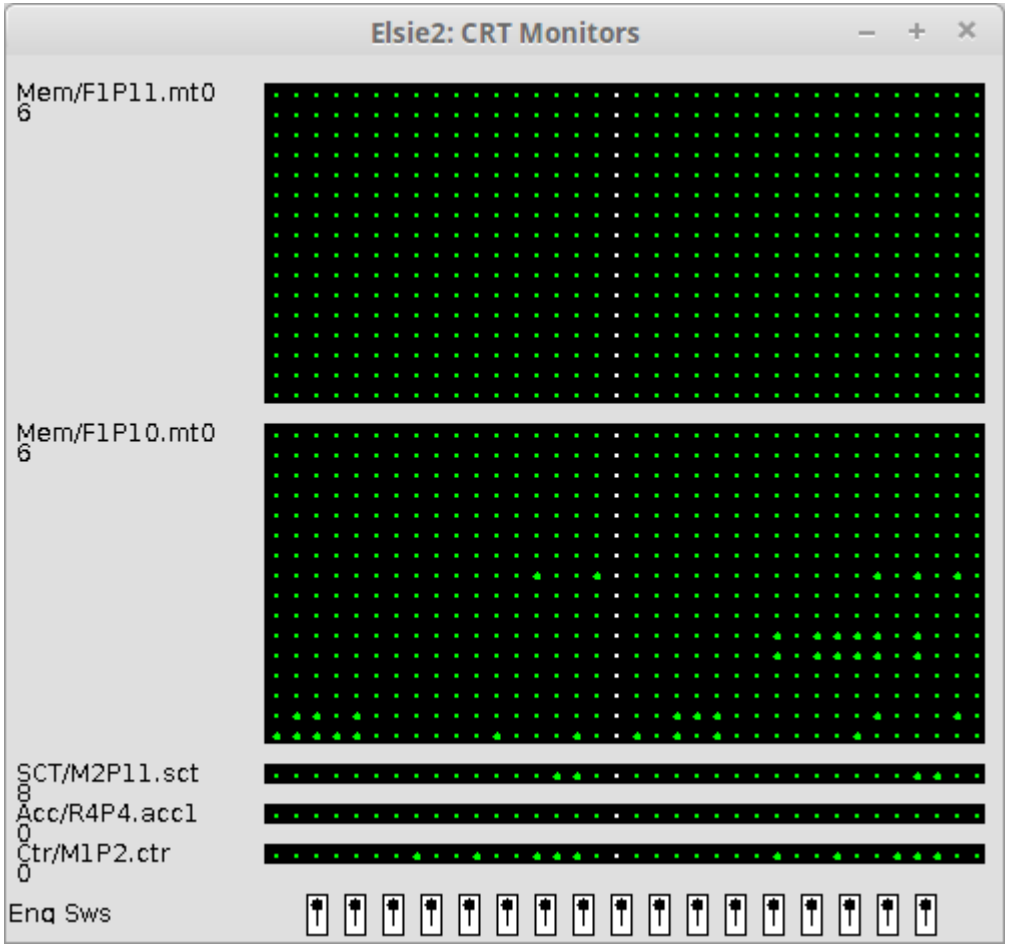
65,77

Next step: Simulation

ELSIE simulates EDSAC devices

Time step fixed at 80nSec,
25 time steps = 1 EDSAC clock pulse


Elsie4.2: Scope Traces: test8a: muladd + +
9216us
128c
127C1P23
pulse Adder-Sum @ 131C14P14 wd 1614 ht 0%
MCU/M1P8+9+10.S1.A
MCU/M1P8+9+10.S2.A
CU/M2P10.Rpulse.A
MCU/M1P8+9+10.R2.A
CCU6/R5P8.EP.A
MCU/M1P8+9+10.G12.A
MCU/M1P8+9+10.G13.A
CU/M2P10.CG+.A
XFR/M1P12.MOB.A
XFR/M1P12.MIB.A
Ctr/M1P2.Counter.A
SCT/M2P11.SCT.A
Order/M2P11.Order~.A
Acc/R4P4.Acc1.A
Acc/R4P4.Acc2.A
ASU2/R3P2.Adder-A.A
CmpCol/R3P10+11.Adder-B.A
Adder/R3P8.Adder-Sum.A
Mpier/R4P11.Mpier.A
Mcand/R4P13.Mcand~.A
TCT/R4P6.Dx.A
TCT/R4P6.Dy.A


Elsie2: CRT Monitors
Mem/F1P11.mt0
6
Mem/F1P10.mt0
6
SCT/M2P11.sct
8
Acc/R4P4.acc1
0
Ctr/M1P2.ctr
0
Enq Sws

Gate-level simulation, very slow!

Run very short test programs

Sufficient to establish confidence that the logic should work

Used as a basis for detailed circuit design

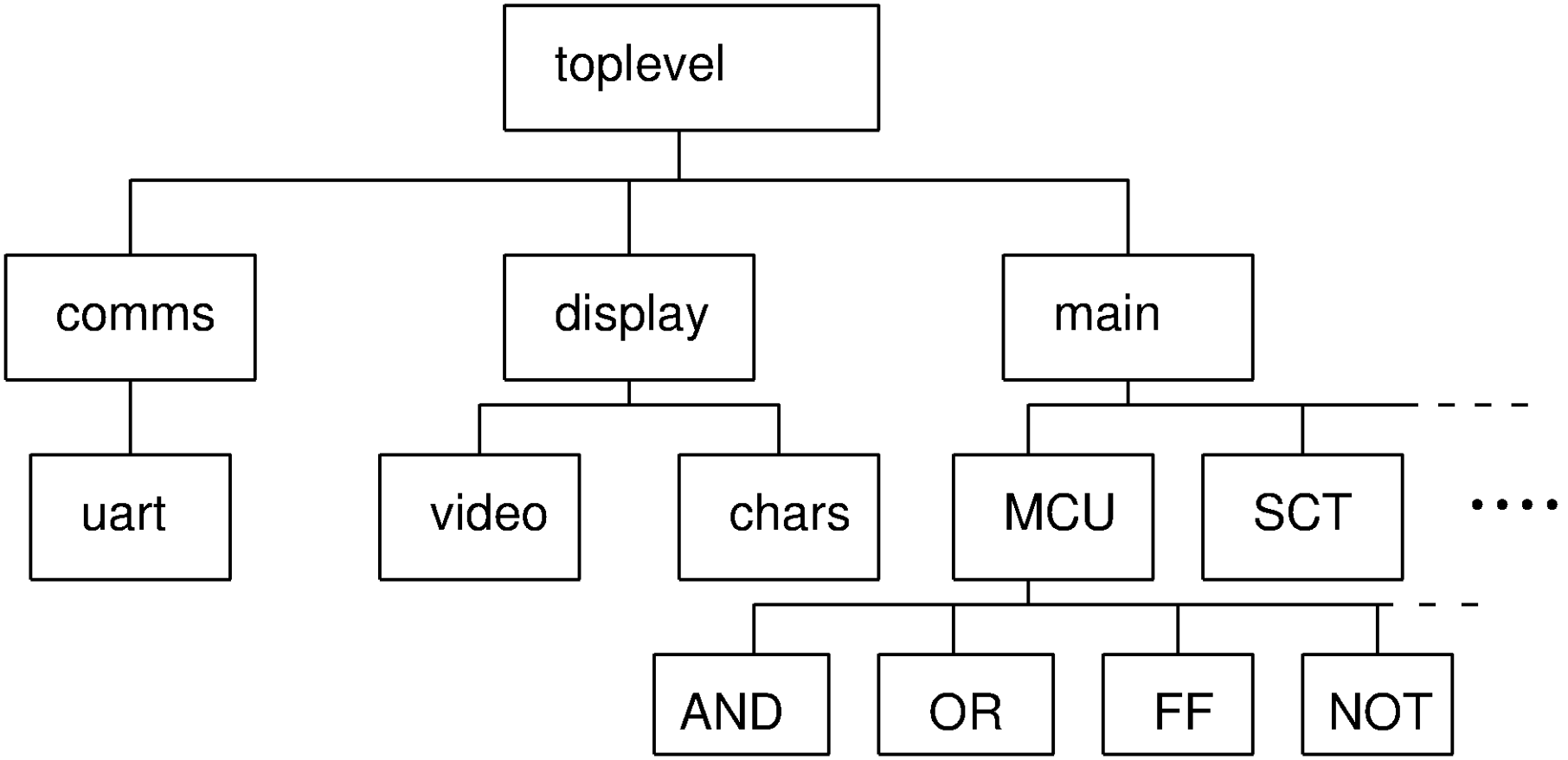
Suggestion that a Verilog implementation might be useful

Offer of Altera DE2 development board
(Simon Moore, Cambridge University)

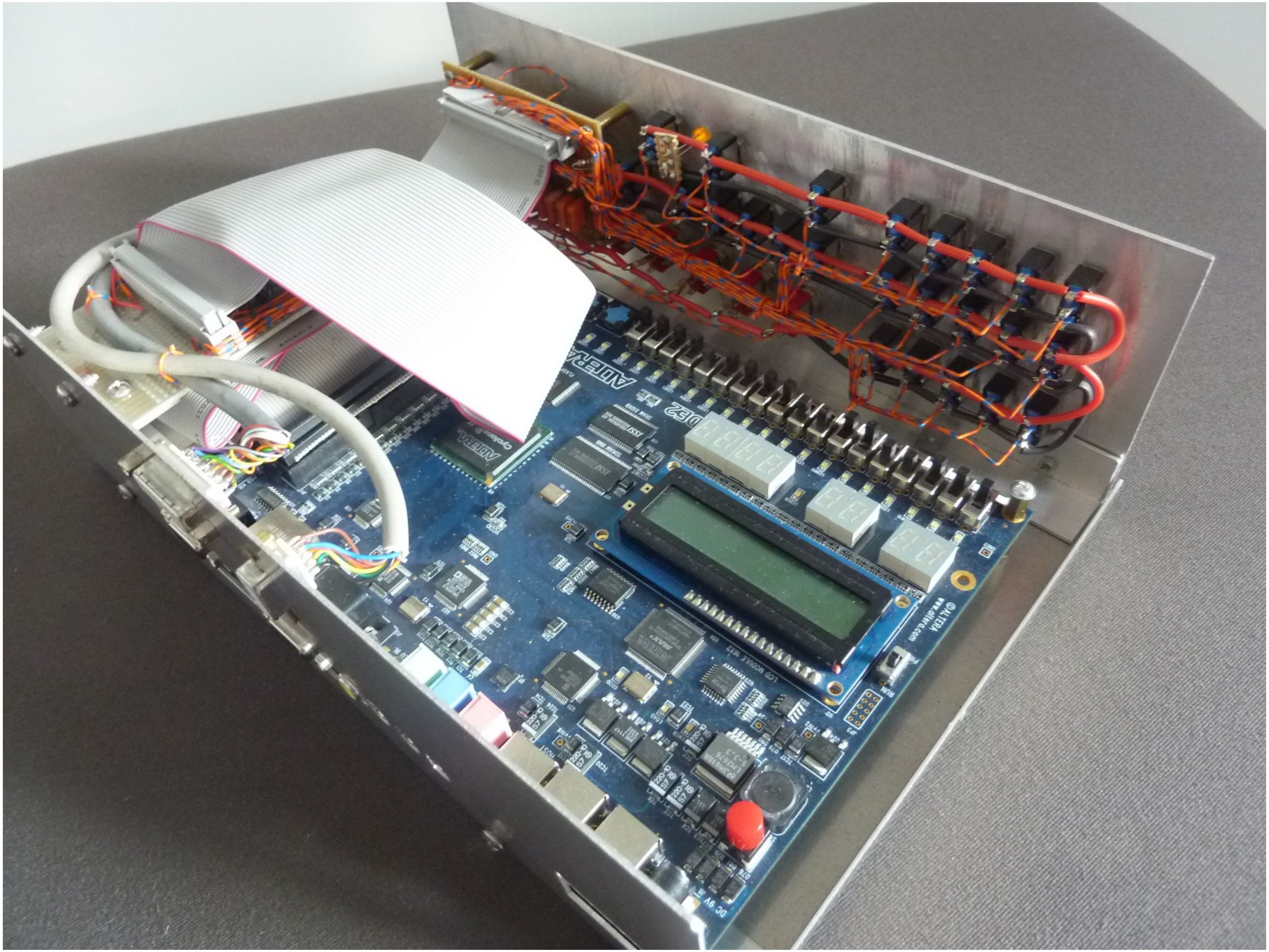
Modify ELSIE to export suitable Verilog code

Hand code Verilog to simulate EDSAC elements and ancilliary modules for I/O and display.

Build board into case with switches etc.


toplevel
comms
display
main
uart
video
chars
MCU
SCT
AND
OR
FF
NOT


512 256 128 64 32
Start Resume SingleEP CLS Stop
Trace Reset



RS232 link to PC/Raspberry Pi for virtual I/O devices:

- Virtual Paper Tape Reader
- Virtual Teleprinter

SVGA port for memory/register displays

Real tape reader added

Real teleprinter still pending

Reimplenting with Altera DE2-115 board

Bigger FPGA, Touch Screen

Work in progress, display, button, but no VIO yet

Mini-EDSAC

Initial version for IceStick

Reduce to 16-bit architecture (from 35-bit)

Simplify some orders

Switch to ASCII tape coding

Register-level coding, not gate-level

Parallel not serial!

Migrate to BlackIce board

Needed external UART for RS232

Project proposal 1:

Extend order set to implement B-register extension

- One additional register
- Three additional orders

Project proposal 2:

Extend to full EDSAC simulation:

- Two orders (17-bit) per word (35-bit)
- Original order set
- Serial arithmetic??

Links:

http://www.billp.org/EDSAC

http://www.billp.org/FPGA